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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/736,244	12/15/2003	Chia Yong Poo	2269-4885.1US (01-0253.01	6438

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 04/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/736,244	POO ET AL.
	Examiner	Art Unit
	Alexander O. Williams	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) *3,4,11 and 13-52* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-10 and 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/15/03; 10/1/04;*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *IDS 1/31/05*.

Serial Number: 10/736244 Attorney's Docket #: 2269-4885.1US01-0252.01/US
Filing Date: 12/15/2003; claimed foreign priority to 6/2/2002

Applicant: Poo et al.

Examiner: Alexander Williams

Applicant's election without traverse of species 3, subspecies 3B of Applicant's detailed species listing of figures 7, 11 and 14 (claims 1 to 45), filed 10/1/2004, has been acknowledged. However, claims 3, 11 and 13-45 DO NOT READ on the elected species of figures 7, 11 and 14, therefore will NOT be examined at this time. Claims 1, 2, 4-10 and 12 DOES READ on the elected species and will now be examined.

This application contains claims 3, 11 and 13-45 drawn to an invention non-elected with traverse.

This application contains claims 46 to 52 drawn to an invention non-elected without traverse.

Applicant's Pre-Amendment filed 3/4/2004 has been acknowledged.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 2, 4-10 and 12 are rejected under 35 U.S.C. § 102(b) as being anticipated by Nakatsuka et al. (U.S. Patent # 5,752,182).

1. Nakatsuka et al. (figures 1 to 14) specifically figure 2 show a semiconductor device package **100**, comprising: a semiconductor device including at least one bond pad **114-119** on an active surface **122** thereof; at least one outer connector **108-113** corresponding to the at least one bond pad, the at least one outer connector positioned on a peripheral edge of the semiconductor device and having a height that extends substantially along a height of the peripheral edge; and at least one conductive trace **102-107** extending between the at least one bond pad and the at least one outer connector.

2. The semiconductor device package of claim 1, Nakatsuka et al. further comprising: an insulative layer positioned beneath at least the at least one conductive trace.

4. The semiconductor device package of claim 1, Nakatsuka et al. further comprising: a back side insulative layer substantially covering a back side of the semiconductor device.

5. The semiconductor device package of claim 1, Nakatsuka et al. show wherein the at least one outer connector comprises opposite surfaces exposed at the active surface and a back side of the semiconductor device.

6. The semiconductor device package of claim 5, Nakatsuka et al. show wherein the at least one outer connector comprises a recess extending substantially from one of the opposite surfaces to another of the opposite surfaces.

7. The semiconductor device package of claim 6, Nakatsuka et al. show wherein the recess has a semicylindrical shape.

8. The semiconductor device package of claim 1, Nakatsuka et al. show comprising a plurality of outer connectors.
9. The semiconductor device package of claim 8, Nakatsuka et al. show comprising a plurality of conductive traces that corresponds to at least some of the plurality of outer connectors.
10. The semiconductor device package of claim 9, Nakatsuka et al. show wherein each of the plurality of conductive traces establishes electrical communication between a bond pad of the semiconductor device and a corresponding outer connector of the plurality of outer connectors.
12. The semiconductor device package of claim 8, Nakatsuka et al. show wherein outer connectors of the plurality of outer connectors are positioned adjacent to at least two peripheral edges of the semiconductor device.

Initially, it is noted that the 35 U.S.C. § 103 rejection based on a conductive trace and a outer connector deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally,

favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Claims 1, 2, 4-6, 8-10 and 12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Lam (U.S. Patent # 5,138,115).

1. Lam (figures 1 to 4) specifically figure 4 show a semiconductor device package **100**, comprising: a semiconductor device including at least one bond pad **12,14,16,18** on an active surface **20** thereof; at least one outer connector **40,42,44,46** corresponding to the at least one bond pad, the at least one outer connector positioned on a peripheral edge of the semiconductor device and having a height that extends substantially along a height of the peripheral edge; and at least one conductive trace **40,42,44,46** extending between the at least one bond pad and the at least one outer connector.

2. The semiconductor device package of claim 1, Lam further comprising: an insulative layer **26** positioned beneath at least the at least one conductive trace.

4. The semiconductor device package of claim 1, Lam further comprising: a back side insulative layer **22** substantially covering a back side of the semiconductor device.

5. The semiconductor device package of claim 1, Lam show wherein the at least one outer connector comprises opposite surfaces exposed at the active surface and a back side of the semiconductor device.

6. The semiconductor device package of claim 5, Lam show wherein the at least one outer connector comprises a recess extending substantially from one of the opposite surfaces to another of the opposite surfaces.

8. The semiconductor device package of claim 1, Lam show comprising a plurality of outer connectors.

9. The semiconductor device package of claim 8, Lam show comprising a plurality of conductive traces that corresponds to at least some of the plurality of outer connectors.

10. The semiconductor device package of claim 9, Lam show wherein each of the plurality of conductive traces establishes electrical communication between a bond pad of the semiconductor device and a corresponding outer connector of the plurality of outer connectors.

12. The semiconductor device package of claim 8, Lam show wherein outer connectors of the plurality of outer connectors are positioned adjacent to at least two peripheral edges of the semiconductor device.

Therefore, it would have been obvious to one of ordinary skill in the art to use the outer connector and the conductive trace as "merely a matter of obvious engineering choice" as set forth in the above case law.

The listed references on USPTO form 892 are cited as of interest to this application.

Field of Search	Date
U.S. Class and subclass: 257/777,686,685,690-693,696,698,673,666,684,796,784,786,787 361/777 174/262,257,52.4,52.2	4/11/05
Other Documentation: foreign patents and literature in 257/	4/11/05
Electronic data base(s): U.S. Patents EAST	4/11/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
9/14/04

Primary Patent Examiner
Alexander O. Williams